R09

Code No: C6303

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I - Semester Examinations, March/April-2011
DIGITAL SIGNAL PROCESSING
(IMAGE PROCESSING)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. a) Verify whether the following systems are linear and time invariant or not
   i) $y(n) = ax(n)$ ii) $y(n) = ax(n-1) + bx(n-2)$
   b) The discrete time systems are represented by the difference equations in which x(n) is the input and y(n) is the output given by $y(n) = x(n+1)-3x(n)+x(n-1)$; $n \geq 0$ check whether the system defined above is linear, time invariant and causal or not. [12]

2. a) Define DFT and IDFT. Compute the DFT of the given time domain sequence $x(n) = \{ 1,2,3,4,4,3,2,1\}$.
   b) List out the properties of DFT with necessary expressions. [12]

3. Develop DIF FFT algorithm for decomposing the DFT for N =12 by considering the factors N = 3.4 and compute for $x(n) = \{1,2,3,4,5,6\}$ [12]

4. a) Define Z- Transform. List out the properties of Z-Transform.
   b) Obtain the Direct form I & II, Parallel and Cascade form realization of the given LTI system governed by the difference equation $y(n) = - 3/8\ Y(n-1) + 3/32\ y(n-2) + 1/64\ y(n-3) + x(n) + 3\ x(n-1) + 2\ x(n-2)$. [12]

5. a) Compare and Contrast Bilinear & Impulse Invariant transformation technique.
   b) Design a Digital Butterworth LPF using bilinear transformation technique for the following specifications
   $0.707 \leq |H(w)| \leq 1 \quad ; 0 \leq w \leq 0.2\pi$
   $|H(w)| \leq 0.08 \ ; 0.4\ \pi \leq w \leq \pi$ [12]

6. a) Compare various windowing techniques w.r.t side-lobes and beam-width.
   b) Design an FIR Digital High pass filter using Hamming window whose cut-off freq is 1.2 rad/s and length of window N = 9. [12]

7. a) What is the importance of Multi-rate Signal Processing and hence define Decimation and Interpolation.
   b) Discuss the sampling rate conversion by a factor I/D with necessary equations. [12]

8. a) Discuss the internal architecture of a TMS 320C54xx Digital signal processor
   b) Explain six stage pipeline architecture of TMS320C54xx processor. [12]

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